

Amendments to the Claims

1 – 16. (Canceled)

17. (Original) A method of forming a CMOS imager, comprising the steps of:

forming an insulating layer over a semiconductor substrate having a photo-collection region;

forming at least one transistor gate over a portion of said insulating layer;

forming an opaque conductive layer over said photo-collection region, said at least one transistor gate and said insulating layer; and

selectively removing said opaque conductive layer from said insulating layer and said photo-collection region.

18. (Original) The method according to claim 17, wherein said photo-collection region includes a photogate.

19. (Original) The method according to claim 17, wherein said transistor gate includes a reset gate.

20. (Original) The method according to claim 19, further comprising a transfer gate.

21. (Original) The method according to claim 17, wherein said transistor gate includes an amplifying transistor.

22. (Original) The method according to claim 21, wherein said amplifying transistor is a source follower transistor.

23. (Original) The method according to claim 20, further comprising a row select gate.

24. (Original) The method according to claim 20, wherein said transfer gate and said reset gate are formed by depositing a doped polysilicon and selectively removing portions of said doped polysilicon to form transistor gates.

25. (Original) The method according to claim 24, wherein said doped polysilicon is selectively removed by etching.

26. (Original) The method according to claim 17, wherein said insulating layer is a silicon dioxide.

27. (Original) The method according to claim 26, wherein said insulating layer is deposited by thermal oxidation of silicon.

28. (Original) The method according to claim 17, wherein said opaque conductive layer is formed by depositing an opaque conductive silicide layer.

29. (Original) The method according to claim 17, wherein said opaque conductive layer is formed by depositing an opaque conductive barrier metal layer.

30. (Original) The method according to claim 28, wherein said opaque conductive silicide layer is a tungsten silicide.

31. (Original) The method according to claim 28, wherein said opaque conductive silicide layer is a titanium silicide.

32. (Original) The method according to claim 28, wherein said opaque conductive silicide layer is a cobalt silicide.

33. (Original) The method according to claim 28, wherein said opaque conductive silicide layer is a molybdenum silicide.

34. (Original) The method according to claim 29, wherein said opaque conductive barrier metal layer is a TiN/W layer.

35. (Original) The method according to claim 29, wherein said opaque conductive barrier metal layer is a WN_x/W layer.

36. (Original) The method according to claim 29, wherein said opaque conductive barrier metal layer is a WN_x layer.

37. (Original) The method according to claim 28, wherein said opaque conductive layer silicide layer is deposited by chemical vapor deposition.

38. (Original) The method according to claim 28, wherein said opaque conductive layer silicide layer is deposited by sputtering.

39. (Original) The method according to claim 29, wherein said opaque conductive barrier layer is deposited by chemical vapor deposition.

40. (Original) The method according to claim 29, wherein said opaque conductive barrier layer is deposited by sputtering.

41. (Original) The method according to claim 17, wherein said opaque conductive layer is selectively removed by etching.

42. (Original) The method according to claim 17, wherein a ring portion of opaque conductive layer remains over an outer periphery of said photo-collection region.

43. (Original) The method according to claim 42, further including adding a light shield over a portion of said imager.

44. (Original) A method of forming a CMOS imager, comprising the steps of:

forming an insulating layer over a semiconductor substrate having a doped photocollection region;

depositing a doped polysilicon layer over said insulating layer;

depositing a photocollection insulator over said photocollection region;

forming an opaque conductive layer over said doped polysilicon layer;

and

patterning said imager to form at least one gate stack having said opaque conductive layer over said gate stack.

45. (Original) The method according to claim 44, wherein said photo-collection region includes a photogate.

46. (Original) The method according to claim 44, wherein said transistor gate stacks include a reset gate.

47. (Original) The method according to claim 46, further comprising a transfer gate stack.

48. (Original) The method according to claim 47, further comprising a row select gate stack.

49. (Original) The method according to claim 44, wherein said transistor gates include an amplifying transistor gate stack.

50. (Original) The method according to claim 49, wherein said amplifying transistor is a source follower transistor gate stack.

51. (Original) The method according to claim 47, wherein said transfer gate and said reset gate are formed by depositing a mask and resist and selectively removing a

portion of said opaque conductive layer, said doped polysilicon layer to form transistor gates.

52. (Original) The method according to claim 51, wherein said layers are selectively removed by etching.

53. (Original) The method according to claim 44, wherein said insulating layer is a silicon dioxide.

54. (Original) The method according to claim 53, wherein said insulating layer is deposited by thermal oxidation of silicon.

55. (Original) The method according to claim 44, wherein said opaque conductive layer is formed by depositing an opaque conductive silicide layer.

56. (Original) The method according to claim 44, wherein said opaque conductive layer is formed by depositing an opaque conductive barrier metal layer.

57. (Original) The method according to claim 55, wherein said opaque conductive silicide layer is a tungsten silicide.

58. (Original) The method according to claim 55, wherein said opaque conductive silicide layer is a titanium silicide.

59. (Original) The method according to claim 55, wherein said opaque conductive silicide layer is a cobalt silicide.

60. (Original) The method according to claim 55, wherein said opaque conductive silicide layer is a molybdenum silicide.

61. (Original) The method according to claim 56, wherein said opaque conductive barrier metal layer is a TiN/W layer.

62. (Original) The method according to claim 56, wherein said opaque conductive barrier metal layer is a WN_x /W layer.

63. (Original) The method according to claim 56, wherein said opaque conductive barrier metal layer is a WN_x layer.

64. (Original) The method according to claim 55, wherein said opaque conductive layer silicide layer is deposited by chemical vapor deposition.

65. (Original) The method according to claim 55, wherein said opaque conductive layer silicide layer is deposited by sputtering.

66. (Original) The method according to claim 56, wherein said opaque conductive barrier layer is deposited by chemical vapor deposition.

67. (Original) The method according to claim 56, wherein said opaque conductive barrier layer is deposited by sputtering.

68. (Original) The method according to claim 44, wherein said silicide is selectively removed by etching.

69. (Original) The method according to claim 44, wherein a ring portion of opaque conductive layer remains over an outer periphery of said photo-collection region.

70. (Original) The method according to claim 69, further including adding a light shield over a portion of said imager.

71 - 86. (Canceled)

87. (New) A CMOS imager having improved transistor speed comprising:

a substrate doped to a first conductivity type;

an array of pixel cells formed on said substrate, each of said cells including a photocollection region doped to a second conductivity type, at least one transistor, and a partially removed opaque conductive layer, wherein said transistor includes, over a gate region of the transistor, a remaining portion of said opaque conductive layer, and said photocollection region includes a photogate from which said opaque conductive layer has been removed; and

signal processing circuitry on said substrate, wherein said circuitry is connected to said array.

88. (New) The CMOS imager according to claim 87, wherein said opaque conductive layer is an opaque conductive silicide layer.

89. (New) The CMOS imager according to claim 87, wherein said opaque conductive layer is an opaque conductive barrier metal layer.

90. (New) The CMOS imager according to claim 88, wherein said opaque conductive silicide layer is a tungsten silicide.

91. (New) The CMOS imager according to claim 88, wherein said opaque conductive silicide layer is a titanium silicide.

92. (New) The CMOS imager according to claim 88, wherein said opaque conductive silicide layer is a cobalt silicide.

93. (New) The CMOS imager according to claim 88, wherein said opaque conductive silicide layer is a molybdenum silicide.

94. (New) The CMOS imager according to claim 89, wherein said opaque conductive barrier metal layer is a TiN/W layer.

95. (New) The CMOS imager according to claim 89, wherein said opaque conductive barrier metal layer is a WN_x/W layer.

96. (New) The CMOS imager according to claim 89, wherein said opaque conductive barrier metal layer is a WN_x layer.

97. (New) The CMOS imager according to claim 87, wherein said transistor is one or more of a reset transistor, a row select transistor, source follower transistor, amplifier transistor or a transfer transistor.

98. (New) The CMOS imager according to claim 87, wherein said transistor is a reset transistor.

99. (New) The CMOS imager according to claim 98, further comprising a transfer transistor to transfer charge from said photocollection region to said signal processing circuitry, wherein said transfer transistor includes an opaque conductive layer deposited over the gate region of said transistor.

100. (New) The CMOS imager according to claim 87, wherein said imager further includes a thin ring of opaque conductive layer formed over the outer periphery of said photogate.

101. (New) The CMOS imager according to claim 100, wherein said imager further includes a light shield formed over said imager such that said light shield does not cover a substantial portion of said photocollection region.

102. (New) A processing system comprising:

(i) a processor; and

(ii) a CMOS imaging device coupled to said processor and including:

a substrate doped to a first conductivity type;

an array of pixel cells formed on said substrate, each of said cells including a photocollection region doped to a second conductivity type, at least one transistor, and a partially removed opaque conductive layer, wherein said transistor includes, over a gate region of the transistor, a remaining portion of said opaque conductive layer, and said photocollection region includes a photogate from which said opaque conductive layer has been removed; and

signal processing circuitry on said substrate, wherein said circuitry is connected to said array.

103. (New) The system according to claim 102, wherein said opaque conductive layer is an opaque conductive silicide layer.

104. (New) The system according to claim 102, wherein said opaque conductive layer is an opaque conductive barrier metal layer.

105. (New) The system according to claim 103, wherein said opaque conductive silicide layer is a tungsten silicide.

106. (New) The system according to claim 103, wherein said opaque conductive silicide layer is a titanium silicide.

107. (New) The system according to claim 103, wherein said opaque conductive silicide layer is a cobalt silicide.

108. (New) The system according to claim 103, wherein said opaque conductive silicide layer is a molybdenum silicide.

109. (New) The system according to claim 104, wherein said opaque conductive barrier metal layer is a TiN/W layer.

110. (New) The system according to claim 104, wherein said opaque conductive barrier metal layer is a WN_x/W layer.

111. (New) The system according to claim 104, wherein said opaque conductive barrier metal layer is a WN_x layer.

112. (New) The system according to claim 102, wherein said transistor is one or more of a reset transistor, a row select transistor, an amplifying transistor, a source follower transistor or a transfer transistor.

113. (New) The system according to claim 102, wherein said transistor is a reset transistor.

114. (New) The system according to claim 113, further comprising a transfer transistor to transfer charge from said photocollection region to said signal processing circuitry, wherein said transfer transistor includes an opaque conductive layer deposited over the gate region of said transistor.

115. (New) The system according to claim 102, wherein said imager further includes a thin ring of opaque conductive layer formed over the outer periphery of said photogate.

116. (New) The system according to claim 115, wherein said imager further includes a light shield formed over said imager such that said light shield does not cover a substantial portion of said photocollection region.

117. (New) A CMOS imager having improved transistor speed comprising:

a substrate doped to a first conductivity type;

an array of pixel cells formed on said substrate, each of said cells including a photocollection region doped to a second conductivity type with an etched photogate, and at least one transistor having a portion of a deposited opaque conductive layer over a gate region of the transistor; and

signal processing circuitry on said substrate, wherein said circuitry is connected to said array,

wherein said photogate is void of said deposited opaque conductive layer.

118. (New) A processing system comprising:

(i) a processor; and

(ii) a CMOS imaging device coupled to said processor and including:

a substrate doped to a first conductivity type;

an array of pixel cells formed on said substrate, each of said cells including a photocollection region doped to a second conductivity type with an etched photogate, and at least one transistor having a portion of a deposited opaque conductive layer over a gate region of the transistor; and

signal processing circuitry on said substrate, wherein said circuitry is connected to said array,

wherein said photogate is void of said deposited opaque conductive layer.

119. (New) A CMOS imager having improved transistor speed comprising:

a substrate; and

an array of pixel cells formed on said substrate, each of said cells including a photogate, a transfer gate, a reset gate, and a partially removed opaque conductive layer, wherein a remaining portion of said opaque conductive layer remains over said transfer gate and said reset gate, and wherein said photogate is void of said opaque conductive layer.

120. (New) The CMOS imager according to claim 119, wherein said opaque conductive layer is an opaque conductive silicide layer.

121. (New) The CMOS imager according to claim 119, wherein said opaque conductive layer is an opaque conductive barrier metal layer.

122. (New) The CMOS imager according to claim 120, wherein said opaque conductive silicide layer is a tungsten silicide.

123. (New) The CMOS imager according to claim 120, wherein said opaque conductive silicide layer is a titanium silicide.

124. (New) The CMOS imager according to claim 120, wherein said opaque conductive silicide layer is a cobalt silicide.

125. (New) The CMOS imager according to claim 120, wherein said opaque conductive silicide layer is a molybdenum silicide.

126. (New) The CMOS imager according to claim 121, wherein said opaque conductive barrier metal layer is a TiN/W layer.

127. (New) The CMOS imager according to claim 121, wherein said opaque conductive barrier metal layer is a WN_x/W layer.

128. (New) The CMOS imager according to claim 121, wherein said opaque conductive barrier metal layer is a WN_x layer.